

**82C924**

**16-Bit Sound Controller**

**Data Book**

Revision 1.0  
912-3000-031  
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## 16-Bit Sound Controller

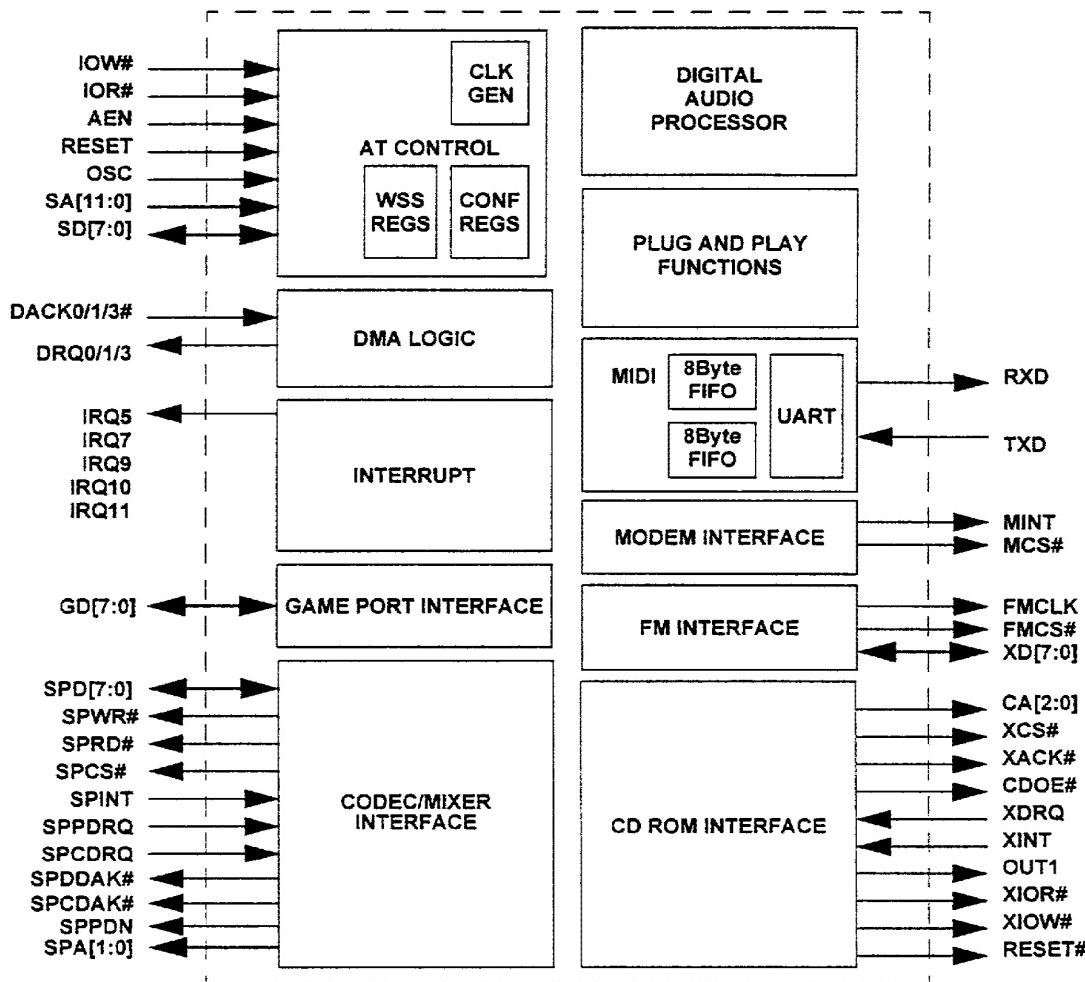
### 1.0 Overview

The OPTi 82C924 is an integrated digital sound controller for PC sound applications. The 82C924 is compatible with Sound Blaster™ Pro, Ad Lib™, MPU-401, and Microsoft Windows Sound System™.

The 82C924 16-bit Sound Controller provides all of the digital functions and interfaces for the Sound Blaster Pro-compatible and Microsoft Windows Sound System-compatible card. The 82C924 is intended to provide an integrated audio solution for business audio, educational/entertainment sound and multimedia applications.

The 82C924 includes the functions of AT Bus interface, Sound Blaster Pro-compatible Digital Audio Processor, MIDI interface, Windows Sound System interface, FM synthesizer interface, Wave Table Synthesizer interface, Game Port timer, Codec/Mixer interface, as well as interfaces to four different types of CD-ROM drives. All DMA and interrupt selections are software programmable. The 82C924 provides enough driving capabilities for AT-Bus interfaces and eliminates the need for external buffering. There is also a power-down mode for power-conscious system designs.

**Figure 1-1 Block Diagram**



## 2.0 Features

- Integrated sound controller compatible with
  - Sound Blaster Pro
  - Ad Lib
  - Microsoft Windows Sound System
- Microsoft Plug and Play compatible
  - Supports eight physical devices
- 8 or 16-bit sound data
  - Sound Blaster 8-bit audio up to 44.1KHz stereo
- Windows 8/16-bit audio up to 48KHz stereo
- Integrated MIDI UART with 8-byte FIFO for both in and out with MPU-401 interface
- Direct OPL2/OPL3/OPL4 interface
- Built-In Game Port Timer
- CD ROM interface for:
  - IDE
  - SONY
  - Mitsumi
  - Panasonic
- All interfaces are software programmable including
  - I/O Address
  - IRQ
  - DRQ
- 18mA drivers for direct AT Bus interface
- Power-down mode
- Silence mode to turn off all audio functions
- Volume control push-button interface
- External Modem chip set interface
- 100 pin package

## 2.1 Applications

Together with the Yamaha OPL3 FM synthesis chip and a 16-bit Codec, such as Crystal Semiconductor 4231 or Analog Devices 1846, the 82C924 provides the integrated solution for the following applications:

- 16-bit sound quality Sound Blaster and Windows Sound System compatible card
- 20 voice FM synthesis
- 16-bit CD-quality WAVE audio up to 48KHz stereo
- IDE CD ROM interface
- Four types of CD-ROM interface
- Game port
- MPU-401 and Sound Blaster MIDI interface
- OPL4 or other wave table synthesis upgrade

## 2.2 ISA Plug and Play on 82C924

The OPTi 82C924 supports the ISA Plug and Play (PnP) Specification 1.0a from Intel and Microsoft. After power-up, the 82C924 is isolated from other PnP cards in the host system by the system software. With this mechanism, the I/O address, IRQ and DMA usage of the 82C924 can be configured by the system according to the free resources available. As a result, the chance of getting a resource conflict is minimized.

The PnP function is enabled by pulling pin 55 (SPA1) of the 82C924 to high at power-up. If that pin is not pulled high at power-up, the 82C924 will operate in non-PnP mode.

A PnP configuration sequence is carried out by either the system BIOS supporting PnP or Configuration Manager software of the operating system. It is used to map the various functional blocks (logical devices) within the 82C924 into the host system address space as well as to configure the DMA and IRQ channels. The configuration sequence occurs as follows:

1. The 82C924 is isolated from the system
2. A unique identifier (handle) is programmed into the 82C924 and the resource data is read
3. After the resource requirement and capabilities are determined, the handle is used to assign conflict-free resources by programming the appropriate information into the 82C924 configuration registers a logical device at a time
4. After the configuration registers are programmed, the 82C924 leaves the configuration mode and each logical device is activated individually. The bus interface of each logical device is then enabled.

The 82C924 supports the following logical devices:

- Audio devices: including Sound Blaster Pro, Windows Sound System, and FM synthesis
- Game Port
- MPU-401 MIDI interface
- IDE CD-ROM interface
- Modem interface
- 82C924 Master Control

## 2.3 Modem Interface

The 82C924 includes the modem as a PnP logical device, as well as interface pins to connect to a modem chipset. When PnP is activated, the 82C924 provides the resource configuration for the modem chipset, such as the I/O address range and interrupt level.

The modem interface pins include pin 35 (MCS#), pin 74 (MINT), pin 42 (IRQ3) and pin 41 (IRQ4). If a modem is con-

nected with the 82C924, the joystick port will provide support for only one joystick.

#### **2.4 Push Button Volume Control**

Two of the pins of the joystick interface can be used as volume control push-buttons (pin 36 as volume down, and pin 37 as volume up) so that the speaker volume can be controlled through front panel buttons in desktop or notebook PCs. Appropriate software drivers are needed to enable this feature.

When the volume control feature is enabled, only one joystick will be supported by the joystick port.

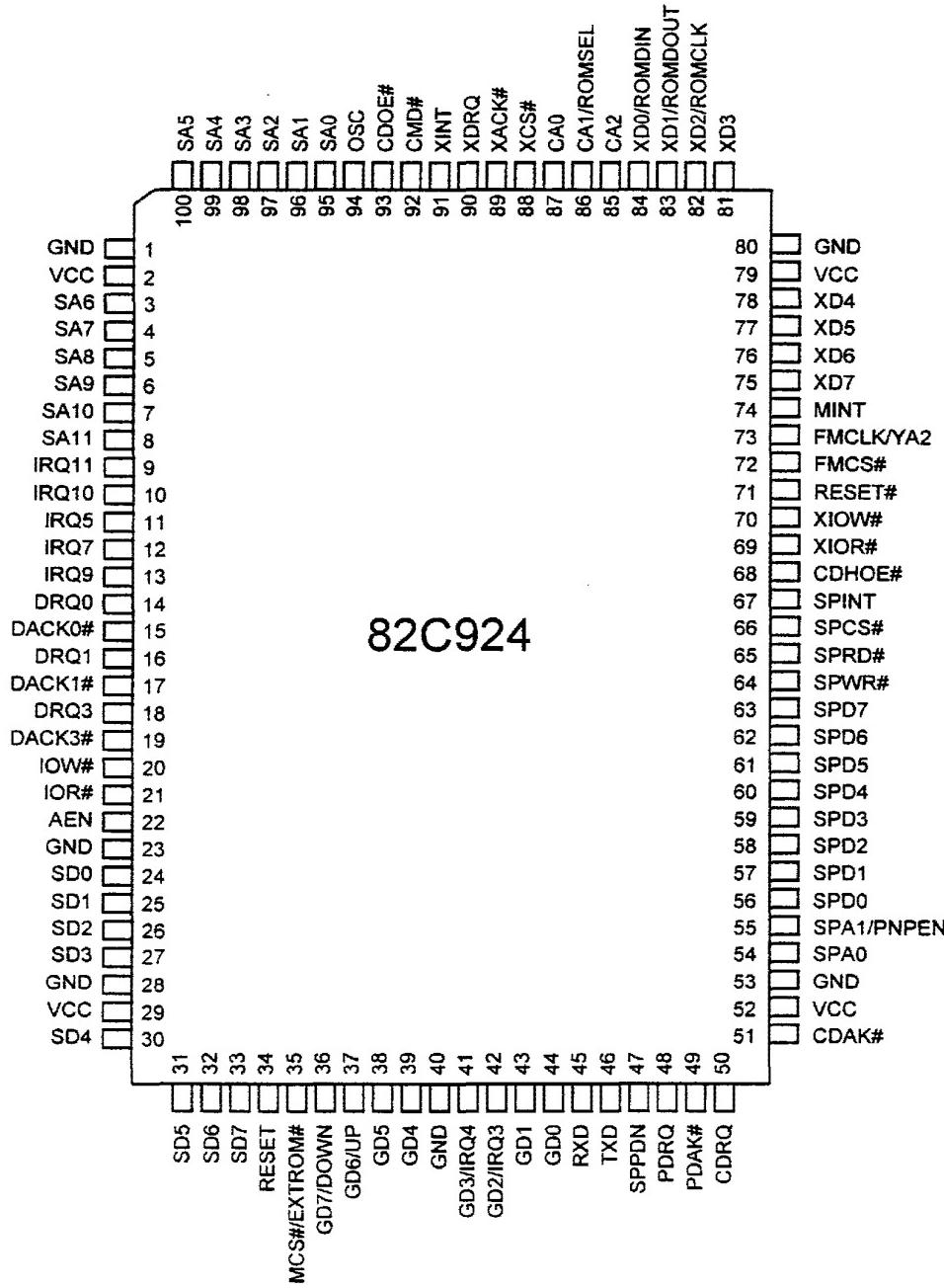
#### **2.5 External Serial EEPROM**

The OPTi 82C924 has the resource data and serial identifier required by the PnP specification stored internally. If the OEM customer wants to use a different resource data and serial identifier to customize their application, an external EEPROM can be used. To use an external EEPROM, pin 35 has to be pulled low. Then the resource data and serial identifier will be read from the external EEPROM instead of the 82C924 internal storage.

The OPTi 82C924 provides a serial EEPROM interface that is compatible with devices from a number of vendors. A 512-byte EEPROM is sufficient for information required by PnP. Pin 82 of the 82C924 provides the data clock for the EEPROM. Pin 83 provides data to the EEPROM, while pin 84 gets input from the EEPROM.

## 3.0 Signal Description

Figure 3-1 Pin Diagram



**Table 3-1 Numerical Pin List**

| Pin | Name   | Pin | Name         | Pin | Name       | Pin | Name        |
|-----|--------|-----|--------------|-----|------------|-----|-------------|
| 1   | GND    | 26  | SD2          | 51  | CDAK#      | 76  | XD6         |
| 2   | VCC    | 27  | SD3          | 52  | VCC        | 77  | XD5         |
| 3   | SA6    | 28  | GND          | 53  | GND        | 78  | XD4         |
| 4   | SA7    | 29  | VCC          | 54  | SPA0       | 79  | VCC         |
| 5   | SA8    | 30  | SD4          | 55  | SPA1/PNPEN | 80  | GND         |
| 6   | SA9    | 31  | SD5          | 56  | SPD0       | 81  | XD3         |
| 7   | SA10   | 32  | SD6          | 57  | SPD1       | 82  | XD2/ROMCLK  |
| 8   | SA11   | 33  | SD7          | 58  | SPD2       | 83  | XD1/ROMDOUT |
| 9   | IRQ11  | 34  | RESET        | 59  | SPD3       | 84  | XD0/ROMDIN  |
| 10  | IRQ10  | 35  | MCS#/EXTROM# | 60  | SPD4       | 85  | CA2         |
| 11  | IRQ5   | 36  | GD7/DOWN     | 61  | SPD5       | 86  | CA1/ROMSEL  |
| 12  | IRQ7   | 37  | GD6/UP       | 62  | SPD6       | 87  | CA0         |
| 13  | IRQ9   | 38  | GD5          | 63  | SPD7       | 88  | XCS#        |
| 14  | DRQ0   | 39  | GD4          | 64  | SPWR#      | 89  | XACK#       |
| 15  | DACK0# | 40  | GND          | 65  | SPRD#      | 90  | XDRQ        |
| 16  | DRQ1   | 41  | GD3/IRQ4     | 66  | SPCS#      | 91  | XINT        |
| 17  | DACK1# | 42  | GD2/IRQ3     | 67  | SPINT      | 92  | CMD#        |
| 18  | DRQ3   | 43  | GD1          | 68  | CDHOE#     | 93  | CDOE#       |
| 19  | DACK3# | 44  | GD0          | 69  | XIOR#      | 94  | OSC         |
| 20  | IOW#   | 45  | RXD          | 70  | XIOW#      | 95  | SA0         |
| 21  | IOR#   | 46  | TXD          | 71  | RESET#     | 96  | SA1         |
| 22  | AEN    | 47  | SPPDN        | 72  | FMCS#      | 97  | SA2         |
| 23  | GND    | 48  | PDRQ         | 73  | FMCLK/YA2  | 98  | SA3         |
| 24  | SD0    | 49  | PDAK#        | 74  | MINT       | 99  | SA4         |
| 25  | SD1    | 50  | CDRQ         | 75  | XD7        | 100 | SA5         |

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Table 3-2    Alphabetical Pin List

| Pin | Name       |
|-----|------------|
| 22  | AEN        |
| 87  | CA0        |
| 86  | CA1/ROMSEL |
| 85  | CA2        |
| 51  | CDAK#      |
| 68  | CDHOE#     |
| 93  | CDOE#      |
| 50  | CDRQ       |
| 92  | CMD#       |
| 15  | DACK0#     |
| 17  | DACK1#     |
| 19  | DACK3#     |
| 14  | DRQ0       |
| 16  | DRQ1       |
| 18  | DRQ3       |
| 73  | FMCLK/YA2  |
| 72  | FMCS#      |
| 44  | GD0        |
| 43  | GD1        |
| 42  | GD2/IRQ3   |
| 41  | GD3/IRQ4   |
| 39  | GD4        |
| 38  | GD5        |
| 37  | GD6/UP     |
| 36  | GD7/DOWN   |

| Pin | Name         |
|-----|--------------|
| 1   | GND          |
| 23  | GND          |
| 28  | GND          |
| 40  | GND          |
| 53  | GND          |
| 80  | GND          |
| 21  | IOR#         |
| 20  | IOW#         |
| 11  | IRQ5         |
| 12  | IRQ7         |
| 13  | IRQ9         |
| 10  | IRQ10        |
| 9   | IRQ11        |
| 35  | MCS#/EXTROM# |
| 74  | MINT         |
| 94  | OSC          |
| 49  | PDAK#        |
| 48  | PDRQ         |
| 34  | RESET        |
| 71  | RESET#       |
| 45  | RXD          |
| 95  | SA0          |
| 96  | SA1          |
| 97  | SA2          |
| 98  | SA3          |

| Pin | Name       |
|-----|------------|
| 99  | SA4        |
| 100 | SA5        |
| 3   | SA6        |
| 4   | SA7        |
| 5   | SA8        |
| 6   | SA9        |
| 7   | SA10       |
| 8   | SA11       |
| 24  | SD0        |
| 25  | SD1        |
| 26  | SD2        |
| 27  | SD3        |
| 30  | SD4        |
| 31  | SD5        |
| 32  | SD6        |
| 33  | SD7        |
| 54  | SPA0       |
| 55  | SPA1/PNPEN |
| 66  | SPCS#      |
| 56  | SPD0       |
| 57  | SPD1       |
| 58  | SPD2       |
| 59  | SPD3       |
| 60  | SPD4       |
| 61  | SPD5       |

| Pin | Name        |
|-----|-------------|
| 62  | SPD6        |
| 63  | SPD7        |
| 67  | SPINT       |
| 47  | SPPDN       |
| 65  | SPRD#       |
| 64  | SPWR#       |
| 46  | TXD         |
| 2   | VCC         |
| 29  | VCC         |
| 52  | VCC         |
| 79  | VCC         |
| 89  | XACK#       |
| 88  | XCS#        |
| 84  | XD0/ROMDIN  |
| 83  | XD1/ROMDOUT |
| 82  | XD2/ROMCLK  |
| 81  | XD3         |
| 78  | XD4         |
| 77  | XD5         |
| 76  | XD6         |
| 75  | XD7         |
| 90  | XDRQ        |
| 91  | XINT        |
| 69  | XIOR#       |
| 70  | XIOW#       |

### 3.1 Signal Definition

I = Input  
 O = Output  
 I/O = Bi-Directional  
 T = Tri-State  
 OD = Open-Drain

#### 3.1.1 AT Bus Signal (36)

| Pin Name   | Pin #           | I/O | I/O Type                  | Function  | To/From |
|------------|-----------------|-----|---------------------------|---|---------|
| IOW#       | 20              | I   | TTL-Smt<br>50KΩ pull-up   | IO Write Command  | AT BUS  |
| IOR#       | 21              | I   | TTL-Smt<br>50KΩ pull-up   | IO Read Command   | AT BUS  |
| AEN        | 22              | I   | TTL-Smt                   | DMA Address Enable  | AT BUS  |
| RESET      | 34              | I   | TTL-Smt<br>50KΩ pull-down | System Reset Input  | AT BUS  |
| OSC        | 94              | I   | TTL                       | AT 14.318MHz Clock  | AT BUS  |
| SA[11:0]   | 8-3,<br>100-95  | I   | TTL                       | System Address  | AT BUS  |
| SD[7:0]    | 33-30,<br>27-24 | I/O | TTL/24mA                  | System Data Bus   | AT BUS  |
| DACK0/1/3# | 15, 17, 19      | I   | TTL<br>50KΩ pull-up       | DMA Acknowledge   | AT BUS  |
| DRQ0/1/3   | 14, 16, 18      | T   | 18mA<br>50KΩ pull-down    | 8-Bit DMA Request   | AT BUS  |
| IRQ5       | 11              | OD  | 18mA<br>5KΩ pull-up       | Interrupt Request   | AT BUS  |
| IRQ7       | 12              | I/O | TTL                       | IRQ7-11 bidirectional for WSS<br>auto interrupt determination |         |
| IRQ9       | 13              |     |                           |   |         |
| IRQ10      | 10              |     |                           |   |         |
| IRQ11      | 9               |     |                           |   |         |

#### 3.1.2 MIDI Interface Signal (2)

| Pin Name | Pin # | I/O | I/O Type | Function      | To/From   |
|----------|-------|-----|----------|---------------|-----------|
| RXD      | 45    | I   | TTL-Smt  | Receive Data  | MIDI Port |
| TXD      | 46    | O   | 18mA     | Transmit Data | MIDI Port |

#### 3.1.3 FM Interface Signal (10)

| Pin Name | Pin # | I/O | I/O Type | Function  | To/From |
|----------|-------|-----|----------|---|---------|
| FMCLK    | 73    | O   | 4mA      | FM Clock Output<br>high during power-down/<br>OPL4 Address[2] | FM      |

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## 3.1.3 FM Interface Signal (10) (cont.)

| Pin Name   | Pin #                       | I/O | I/O Type                 | Function  | To/From |
|--|-----------------------------|-----|--------------------------|---|---------|
| FMCS#  | 72                          | O   | 4mA                      | FM Chip Select,<br>Asserted for IO address<br>SBBBase + 0-3<br>SBBBase + 8-9<br>388-38B | FM      |
| XD[7:3]<br>XD2/ROMCLK<br>XD1/ROMDOUT<br>XD0/ROMDIN | 75-78, 81<br>82<br>83<br>84 | I/O | TTL / 4mA<br>5KΩ pull-up | Local Data Bus  | FM      |

## 3.1.4 CD ROM Interface Signal (13)

| Pin Name   | Pin # | I/O | I/O Type              | Function                           | To/From    |
|------------|-------|-----|-----------------------|------------------------------------|------------|
| CA1/ROMSEL | 86    | O   | 12mA                  | CD ROM Address 1                   | CD ROM     |
| CA0        | 87    | O   | 12mA                  | CD ROM Address 0                   | CD ROM     |
| XCS#       | 88    | O   | 12mA                  | CD ROM Chip Select                 | CD ROM     |
| XACK#      | 89    | I/O | TTL/12mA              | CD ROM DAM Acknowledge             | CD ROM     |
| XDRQ       | 90    | I   | TTL<br>50KΩ pull-down | CD ROM Request                     | CD ROM     |
| XINT       | 91    | I   | TTL<br>50KΩ pull-up   | CD ROM Interrupt Request           | CD ROM     |
| CA2        | 85    | I/O | TTL<br>12mA           | CD ROM Address 2                   | CD ROM     |
| CMD#       | 92    | O   | 12mA                  | Command Output                     | CD ROM     |
| CDOE#      | 93    | O   | 4mA                   | CD data buffer output enable       |            |
| CDHOE#     | 68    | O   | 4mA                   | CD[15:8] data buffer output enable |            |
| XIOR#      | 69    | O   | 12mA                  | Buffered IOR#                      | CD ROM, FM |
| XIOW#      | 70    | O   | 12mA                  | Buffered IOW#                      | CD ROM, FM |
| RESET#     | 71    | O   | 12mA                  | Buffered RESET, active low         | CD ROM, FM |

### 3.1.5 Game Interface Signal (8)

| Pin Name | Pin # | I/O | I/O Type | Function                   | To/From |
|----------|-------|-----|----------|----------------------------|---------|
| GD7/DOWN | 36    | I/O | 4mA      | Game Port Data/Push Button |         |
| GD6/UP   | 37    | I   | TTL      |                            |         |
| GD5      | 38    | I   | TTL      |                            |         |
| GD4      | 39    | I   | TTL      |                            |         |
| GD3/IRQ4 | 41    | I/O | 16mA     | Game Port Data/            |         |
| GD2/IRQ3 | 42    | I/O | CMOS     | Modem Control              |         |
| GD1      | 43    | I/O | Schmitt  |                            |         |
| GD0      | 44    | I/O | PU       |                            |         |

### 3.1.6 Codec/Mixer Signal (19)

| Pin Name   | Pin #  | I/O | I/O Type                | Function                              | To/From |
|------------|--------|-----|-------------------------|---------------------------------------|---------|
| SPA1/PNPEN | 55, 54 | I/O | TTL/4mA<br>50KΩ pull-up | Codec Address<br>Plug and Play Enable |         |
| SPA0       |        |     |                         |                                       |         |
| SPD7-SPD0  | 63-56  | I/O | TTL/4mA<br>50KΩ pull-up | Codec Data                            |         |
| SPWR#      | 64     | O   | 4mA                     | Codec Write Command                   |         |
| SPRD#      | 65     | O   | 4mA                     | Codec Read Command                    |         |
| SPCS#      | 66     | O   | 4mA                     | Codec Chip Select                     |         |
| SPINT      | 67     | I   | TTL                     | Codec Interrupt Request               |         |
| PDRQ       | 48     | I   | TTL                     | Playback DMA Request                  |         |
| CDRQ       | 50     | I   | TTL                     | Capture DMA Request                   |         |
| SPPDN      | 47     | O   | 4mA                     | Codec Power-down, active low          |         |
| PDAK#      | 49     | O   | 4mA                     | Playback DMA Acknowledge              |         |
| CDAK#      | 51     | O   | 4mA                     | Capture DMA Acknowledge               |         |

### 3.1.7 Modem Interface

| Pin Name     | Pin # | I/O | I/O Type | Function                               | To/From |
|--------------|-------|-----|----------|--|---------|
| MCS#/EXTROM# | 35    | I/O | TTL/4mA  | Modem Chip Select/<br>Use External ROM |         |
| MINT         | 74    | I   | TTL      | Modem Interrupt                        |         |

### 3.1.8 Power Pins (10)

| Pin Name | Pin #                 |
|----------|-----------------------|
| Vcc      | 2, 29, 52, 79         |
| GND      | 1, 23, 28, 40, 53, 80 |

## 4.0 Register Description

Table 4-1 Register Map

| I/O Address              | Description   | R/W   |
|--------------------------|---|---|
| SBBase + 0<br>ALBase + 0 | Left FM Status Port                                   | R only                                      |
| SBBase + 0<br>ALBase + 0 | Left FM Register Address Port                         | W only                                      |
| SBBase + 1<br>ALBase + 1 | Left FM Data Port                                     | W only                                      |
| SBBase + 2<br>ALBase + 2 | Right FM Register Address Port                        | W only                                      |
| SBBase + 3<br>ALBase + 3 | Right FM Data Port                                    | W only                                      |
| SBBase + 4               | Mixer Address Port                                    | W only                                      |
| SBBase + 5               | Mixer Data Port                                       | R/W   |
| SBBase + 6               | Digital Audio Processor Software Reset                | W only                                      |
| SBBase + 8               | FM Status Port  | R only                                      |
| SBBase + 8               | FM Register Address Port                              | W only                                      |
| SBBase + 9               | FM Data Port  | W only                                      |
| SBBase + A               | Digital Audio Processor Read Data                     | R only, Digital Audio Processor AO = 0      |
| SBBase + C               | Digital Audio Processor Write Data/Cmd                | W only, Digital Audio Processor AO = 1      |
| SBBase + C               | Digital Audio Processor Write Buffer Status           | R only, Digital Audio Processor AO = 1      |
| SBBase + E               | Digital Audio Processor Output Buffer Status Register | R only, Digital Audio Processor AO = 1      |
| WSBase + 0-3             | Configuration   | W only                                      |
| WSBase + 0-3             | Version   | R only                                      |
| WSBase + 4               | Codec Index Register                                  | R/W, exists in Codec and shadowed in 82C924 |
| WSBase + 5               | Codec Indexed Data Register                           | R/W, exists in Codec only                   |
| WSBase + 6               | Codec Status Register                                 | R/W, exists in Codec only                   |
| WSBase + 7               | Codec Direct Data                                     | R/W, exists in Codec only                   |
| 200-207                  | Game Port   | R/W   |
| CDBase + 0-3             | CD ROM Interface Registers                            | R/W   |
| MCBBase + 3 (\$F8F)      | Password Register                                     | W only                                      |
| MCBBase + 1 (\$F8D)      | MC1   | R/W   |
| MCBBase + 2 (\$F8E)      | MC2   | R/W   |
| MCBBase + 3 (\$F8F)      | MC3   | R/W   |
| MCBBase + 4 (\$F90)      | MC4   | R/W   |

**Table 4-1 Register Map (cont.)**

| I/O Address        | Description       | R/W |
|--------------------|-------------------|-----|
| MCBase + 5 (\$F91) | MC5               | R/W |
| MCBase + 6 (\$F92) | MC6               | R/W |
| MCBase + 7 (\$F93) | MC7               | R/W |
| MCBase + 8 (\$F94) | MC Indirect Index | R/W |
| MCBase + 9 (\$F95) | MC Indirect Data  | R/W |
| MC8                | Indirect Register | R/W |
| MC9                | Indirect Register | R   |
| MC10               | Indirect Register | R   |
| MC11               | Indirect Register | R   |
| MC12               | Indirect Register | R   |
| 279                | PNP Address       | W   |
| A79                | PNP Write_Data    | W   |
| PNPBase            | PNP Read_Data     | R   |

#### 4.1 82C924 Register Definition

##### Mode Control Register 1

Note Password = "E5".

| MC1(F8D) R/W with password, MC1[3:0] jumper initialized |     |                 |   |             |   |   |       |
|---|-----|-----------------|---|-------------|---|---|-------|
| 7   | 6   | 5               | 4 | 3           | 2 | 1 | 0     |
| MOD   | PDN | Sound Base[1:0] |   | CDTYPE[2:0] |   |   | GPEN# |

- MOD:** Operation Mode  
 0 = Sound Blaster compatible mode (default)  
 1 = Windows Sound System compatible
- PDN:** Power-down Mode  
 0 = Disabled  
 1 = Enabled: all internal clocks are stopped and FMCLK is stopped in high level
- Sound Base:** I/O Base Address  
 In Windows Sound System mode, MC[5:4] select the I/O base address among four specified addresses  
 00:WSBase = 530 (default)  
 01:WSBase = E80  
 10:WSBase = F40  
 11:WSBase = 604
- CD Type:** Type of CD ROM interface  
 000: CD Disabled (default)  
 001: SONY 31A  
 010: Mitsumi  
 011: Panasonic  
 100: Secondary IDE  
 101: Reserved  
 110: Reserved  
 111: Chip Test Mode



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GPEN#: Game Port Enable  
0: Enable  
1: Disable

Default = 00h

## Mode Control Register 2

| MC2 (F8E) R/W with password |      |   |       |   |       |   |   |  |
|-----------------------------|------|---|-------|---|-------|---|---|--|
| 7                           | 6    | 5 | 4     | 3 | 2     | 1 | 0 |  |
| CDSEL[1:0]                  | OPL4 |   | CDIRQ |   | CDDRQ |   |   |  |

CDSEL: CD ROM Base Address  
The base I/O address for the CD ROM interface  
00: CD Base = 340h (default)  
01: CD Base = 330h  
10: CD Base = 360h  
11: CD Base = 320h

OPL4: Yamaha OPL4 Synthesis Chip  
0 = OPL3 FM synthesis chip is assumed (default)  
1 = OPL4 Wave Table synthesis chip is assumed

CDIRQ: CD ROM Interrupt Select  
Selects the interrupt channel for the CD ROM interface  
000: CD IRQ = disabled (default)

001: CD IRQ = 5  
010: CD IRQ = 7  
011: CD IRQ = disabled  
100: CD IRQ = 9  
101: CD IRQ = 10  
110: CD IRQ = 11  
111: CD IRQ = disabled

CDDRQ: CD ROM DMA Select  
00: CD DRQ = 3  
01: CD DRQ = 0  
10: CD DRQ = 1  
11: CD DRQ = disabled (default)

Default = 03h

## Mode Control Register 3

| MC3 (F8F) R/W with password |             |   |      |        |               |               |   |  |
|-----------------------------|-------------|---|------|--------|---------------|---------------|---|--|
| 7                           | 6           | 5 | 4    | 3      | 2             | 1             | 0 |  |
| DAIRQ[1:0]                  | DADREQ[1:0] |   | FMAP | DABASE | REV[1]/WRSROM | REV[0]/CMDPAS |   |  |

DAIRQ: Digital Audio Interrupt Request Select for Sound Blaster Mode  
00: IRQ = 7  
01: IRQ = 10  
10: IRQ = 5  
11: IRQ = disabled

DADREQ: Digital Audio DMA Channel Select for Sound Blaster Mode  
00: DRQ = 1  
01: DRQ = 0  
10: DRQ = 3  
11: DRQ = disabled

**FMAP:** Frequency Mapping Select for Sound Blaster Mode  
 0 = Normal Mode: Frequency is mapped to the nearest frequency using both crystals of the Codec  
 1 = Single Mode: Frequency is mapped only to the 16MHz crystal of the Codec

**DATABASE:** DA Base Address  
 0 = 220h  
 1 = 240h

**REV[1]/WRSROM:**  
 Read: Chip ID high bit  
 Write: Enable write to external EPROM

**REV[0]/CMDPAS:**  
 Read: Chip ID low bit  
 Write: Enable passing of Sound Blaster command when DRQ is active

Default = F2h

#### Mode Control Register 4

| MC4 (F90) |       |          |           |       |         |       |   |
|-----------|-------|----------|-----------|-------|---------|-------|---|
| 7         | 6     | 5        | 4         | 3     | 2       | 1     | 0 |
| ADPCMEN   | GPOUT | ACKSIMEN | PNP MODE# | FMCLK | SILENCE | SBVER |   |

**ADPCMEN:** Sound Blaster ADPCM Enable, reserved, must be 1

**GPOUT:** General Purpose Output

**ACKSIMEN:** Time Out ACK Enable. Reserved must be 1

**PNP MODE#:** Reserved

0 = PNP Mode

1 = 929 mode for older game compatibility

**FMCLK:** OPLx Clock Output Enable

0 = OPL3

1 = OPL2

**SILENCE:** Audio Interface Enable

0 = Enabled

1 = Disabled

**SBVER:** Sound Blaster Version

00: Version 2.1

01: Version 1.5

10: Version 3.2

11: Version 4.4

Default = A2h

#### Mode Control Register 5

| MC5 (F91) |      |        |          |       |      |      |         |
|-----------|------|--------|----------|-------|------|------|---------|
| 7         | 6    | 5      | 4        | 3     | 2    | 1    | 0       |
| AVCEN#    | OPL5 | SHPASS | SBACCESS | CFIFO | EPEN | CFIX | CDFTOEN |

**AVCEN#:** Automatic Volume Control, active low

0 = Enable

1 = Disable

**OPL5:** OPL5 Address Decoding, reserved

1 = Select the OPL5 address decoding

**SHPASS:** Write Protect Internal CODEC Shadow Registers

0 = Not protected

1 = Protected



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**SBACCESS:** Set Codec Access in Sound Blaster Mode  
0 = Disabled  
1 = Enabled  
**CFIFO:** Set Command FIFO in Sound Blaster Mode, write only  
**EPEN:** Must be 1  
**CFIX:** Enable fix for Crystal 4248/4231 Synchronization Delays  
0 = AD 1848  
1 = CS4231  
**CDFTOEN:** Must be 1  
Default = 2F

## Mode Control Register 6 - MIDI Interface

| MC6 (F92) Write Only |            |   |             |   |          |          |         |
|----------------------|------------|---|-------------|---|----------|----------|---------|
| 7                    | 6          | 5 | 4           | 3 | 2        | 1        | 0       |
| MPU-401              | MPU-401 BA |   | MPU-401 INT |   | DRQTM EN | AUDIO EN | ATTN EN |

**MPU-401:** Select MPU-401  
0 = Disable  
1 = Enable

**MPU-401 BA:** MPU Base Address Select  
00 = 330h  
01 = 320h  
10 = 310h  
11 = 300h

**MPU-401 INT:** Interrupt Select  
00 = IRQ9  
01 = IRQ10  
10 = IRQ5  
11 = IRQ7

**DRQTM EN:** DMA Watch Dog Enable  
0 = Disable  
1 = Enable

**AUDIO EN:** 0 = Disable WAVE  
1 = Enable WAVE

**ATTN EN:** Must be 1  
Default = 83h

## Mode Control Register 7 - Volume

| MC7 (F93) |          |         |       |       |       |       |       |
|-----------|----------|---------|-------|-------|-------|-------|-------|
| 7         | 6        | 5       | 4     | 3     | 2     | 1     | 0     |
| VCINT EN  | PNP TEST | MC MUTE | ATTN4 | ATTN3 | ATTN2 | ATTN1 | ATTN0 |

**VCINT EN:** Volume Control Interrupt Enable

**PNP TEST:** PNP Test Mode

**MC MUTE:** Mute WAVE Output

**ATTN[4:0]:** WAVE Volume Adjustment

When WRSROM (MC3[1]) is active, ATTN [2:0] are used to write to external EPROM, as follows:

ATTN0 = ROMDOUT

ATTN1 = SROMCLK

ATTN2 = SROMCS



**Mode Control Register 8**

| MC8 (indirect) |   |   |             |   |   |          |   |
|----------------|---|---|-------------|---|---|----------|---|
| 7              | 6 | 5 | 4           | 3 | 2 | 1        | 0 |
| Reserved       |   |   | VCISEL[1:0] |   |   | Reserved |   |

MC8[7:5]: Reserved

VCISEL[1:0]: Volume Control Interrupt Select

00 = Disable

01 = IRQ5

10 = IRQ10

11 = IRQ11

MC8[2:0]: Reserved

**Mode Control Register 9**

| MC9 (indirect) Read Only |   |       |   |   |          |   |   |
|--------------------------|---|-------|---|---|----------|---|---|
| 7                        | 6 | 5     | 4 | 3 | 2        | 1 | 0 |
| Reserved                 |   | ROMIN |   |   | Reserved |   |   |

MC9[7:6]: Reserved

ROMIN: External EEPROM data in.

MC9[4:0]: Reserved

**Mode Control Register 10**

| MC10 (indirect) Read Only |   |   |   |   |   |   |   |
|---------------------------|---|---|---|---|---|---|---|
| 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved                  |   |   |   |   |   |   |   |

MC10[7:0]: Reserved

**Mode Control Register 11**

| MC11 (indirect) Read Only |   |   |   |   |   |   |   |
|---------------------------|---|---|---|---|---|---|---|
| 7                         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved                  |   |   |   |   |   |   |   |

MC11[7:0]: Reserved

**Mode Control Register 12**

| MC12 (indirect) Read Only |       |       |         |        |       |          |   |
|---------------------------|-------|-------|---------|--------|-------|----------|---|
| 7                         | 6     | 5     | 4       | 3      | 2     | 1        | 0 |
| IDEEN                     | BUTUP | BUTDN | BUTMUTE | BUTINT | PNPEN | Reserved |   |

IDEEN: IDE CD-ROM device enabled

BUTUP: Volume up button pushed

BUTDN: Volume down button pushed

BUTMUTE: Both up and down buttons pushed

BUTINT: Volume control interrupt pending

PNPEN: Plug and Play mode enabled

MC12[1:0]: Reserved

Note Read of MC12 will clear BUTUP, BUTDN, BUTMUTE, and BUTINT.



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## Mode Control Index Register

### MC Indirect Index (F94)

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |   |   |   |   |   |   |   |

## Mode Control Indirect Data Register

### MC Indirect Data (F95)

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |   |   |   |   |   |   |   |

## DAP Registers

### Digital Audio Processor Reset (SBBBase+C) Write Only

|              |   |   |   |   |   |   |       |
|--------------|---|---|---|---|---|---|-------|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| "Don't care" |   |   |   |   |   |   | RESET |

RESET = '1' will perform a software reset on the Digital Audio Processor at the end of the IO write command. It actually sets a software reset flag. This software reset is terminated by performing another write at this location with RESET = '0'. A system reset will reset the software reset flag and thus terminates the software reset.

### Digital Audio Processor Read Data (SBBBase+A) Read Only

|      |   |   |   |   |   |   |   |
|------|---|---|---|---|---|---|---|
| 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA |   |   |   |   |   |   |   |

This is the data output port of the Digital Audio Processor.

### Digital Audio Processor Write Buffer Status (SBBBase+C) Read Format

|        |                  |   |   |   |   |   |   |
|--------|------------------|---|---|---|---|---|---|
| 7      | 6                | 5 | 4 | 3 | 2 | 1 | 0 |
| IBFULL | (SBBBase+A)[6:0] |   |   |   |   |   |   |

IBFULL is '1' when the Digital Audio Processor Input Buffer is full. This flag is set when the host CPU writes data in the input data bus buffer and cleared when the data is read by the internal Digital Audio Processor.

### Digital Audio Processor Data/Command Register (SBBBase+C) Write Format

|              |   |   |   |   |   |   |   |
|--------------|---|---|---|---|---|---|---|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Command/Data |   |   |   |   |   |   |   |

This is the data/command write port for the Digital Audio Processor.

### Digital Audio Processor Output Buffer Status (SBBBase+E) Read Only

|        |                     |   |   |   |   |   |   |
|--------|---------------------|---|---|---|---|---|---|
| 7      | 6                   | 5 | 4 | 3 | 2 | 1 | 0 |
| OBFULL | Output Buffer [6:0] |   |   |   |   |   |   |

OBFULL = 1 when the Digital Audio Processor Output Buffer is full. This flag is set in the Digital Audio Processor when data is written in the output data bus buffer and cleared when the host CPU or the DMA controller reads the data in the output data bus buffer.

Reading this register will also clear the Digital Audio Processor interrupt request.

**WSS Configuration Register**

| WSBase+0-3 Write Only |     |       |   |   |   |   |       |  |
|-----------------------|-----|-------|---|---|---|---|-------|--|
| 7                     | 6   | 5     | 4 | 3 | 2 | 1 | 0     |  |
| Reserved              | ISS | WSIRQ |   |   |   |   | WSDRQ |  |

ISS: IRQ Sense Source

0 = Normal

1 = Auto-Interrupt Selection

WSIRQ: IRQ Select

000 = Disabled

001 = IRQ7

010 = IRQ9

011 = IRQ10

100 = IRQ11

101, 110, 111 = Reserved

WSDRQ: DMA Request Select

|     | Playback | Capture  |
|-----|----------|----------|
| 000 | Disabled | Disabled |
| 001 | DRQ0     | Disabled |
| 010 | DRQ1     | Disabled |
| 011 | DRQ3     | Disabled |
| 100 | Disabled | DRQ1     |
| 101 | DRQ0     | DRQ1     |
| 110 | DRQ1     | DRQ0     |
| 111 | DRQ3     | DRQ0     |

**WSS Version Register**

| WSBase+0-3 Read Only |          |         |   |   |   |   |   |  |
|----------------------|----------|---------|---|---|---|---|---|--|
| 7                    | 6        | 5       | 4 | 3 | 2 | 1 | 0 |  |
| CHANNEL              | IRQSENSE | VERSION |   |   |   |   |   |  |

CHANNEL: Channel Available

0 = DRQ0/1/3 and IRQ7/9/10/11 available

1 = DRQ1/3 and IRQ7/9 available

IRQSENSE: 0 = No interrupt

1 = WSS interrupt active

VERSION: 04h

## 5.0 Electrical Specification

### 5.1 Absolute Maximum Ratings

| Sym. | Description         | Min  | Max       | Units |
|------|---------------------|------|-----------|-------|
| VDD  | Supply Voltage      | -0.5 | 6.5       | V     |
| VI   | Input Voltage       | -0.5 | VDD + 0.5 | V     |
| VO   | Output Voltage      | -0.5 | VDD + 0.5 | V     |
| TSTG | Storage Temperature | -40  | 125       | °C    |
|      | Power Dissipation   | TBD  | TBD       | V     |

### 5.2 Recommended DC Operating Conditions

| Sym. | Description           | Min  | Max  | Units |
|------|-----------------------|------|------|-------|
| VDD  | Supply Voltage        | 4.5  | 5.5  | V     |
| AVD  | Supply Voltage        | 4.75 | 5.25 | V     |
| TOP  | Operating Temperature | 0    | 70   | °C    |

### 5.3 General Specification (VDD = 5.0V)

| Sym. | Description                      | Condition              | Min        | Typ.       | Max        | Units |
|------|----------------------------------|------------------------|------------|------------|------------|-------|
| IIL  | Low Level Input Current          | VIN = VSS              | -10        |            | +10        | uA    |
| IIH  | High Level Input Current         | VIN = VDD              | -10        |            | +10        | uA    |
| IOZ  | Tri-State Output Leakage Current | VOUT = 0/VDD           | -10        |            | +10        | uA    |
| V-   | Schmitt Negative Threshold       | TTL-STATIC CMOS-STATIC | 0.8<br>1.5 |            | 1.3<br>2.5 | V     |
| V+   | Schmitt Positive Threshold       | TTL-STATIC CMOS-STATIC | 1.4<br>2.5 |            | 2.1<br>3.5 | V     |
| VH   | Schmitt Hysteresis               | TTL-STATIC CMOS-static |            | 0.6<br>1.0 |            | V     |
| VIL  | low Level Input Voltage          | TTL-STATIC             |            |            | 0.8        | V     |
| VIH  | High Level Input Voltage         | TTL-STATIC             | 2.0        |            |            | V     |
| VOL  | Low Level Output Voltage         | TTL-STATIC             |            |            | 0.4        | V     |
| VOH  | High Level Output Voltage        | TTL-STATIC             | 2.4        |            |            | V     |
| RPD  | Pull-Down Resistance             | VIN = VDD              | 50         |            | 200        | KΩ    |
| RPU  | Pull-Up Resistance               | VIN = Vss              | 50         |            | 200        | KΩ    |
| CIN  | Input Capacitance                | FREQ = 1MHz @ 0V       |            |            | 5          | pF    |
| COUT | Output Capacitance               | FREQ = 1MHz @ 0V       |            |            | 5          | pF    |
| CIO  | Bi-Directional Capacitance       | FREQ = 1MHz @ 0V       |            |            | 5          | pF    |
| Ios  | Short Circuit Output Current     | VOUT = 0V              |            | 2          | 25         | mA    |
| IKLU | I/O Latch-Up Current             | V < Vss, V > VDD       | 100        |            |            | mA    |
| VESD | Electrostatic Protection         | C = 100pF, R = 1.5KΩ   | 2000       |            |            | V     |

## 5.4 Timing Parameters

### 5.4.1 AT Bus Timing

| Description                        | Sym   | Min    | Max    | Units |
|------------------------------------|-------|--------|--------|-------|
| OSC (14.318 MHz) Frequency         | TOSCP | 14.000 | 14.500 | MHz   |
| OSC High Width                     | TOSCH | 32     | 40     | ns    |
| OSC Low Width                      | TOSCL | 32     | 40     | ns    |
| RESET to RST#                      | TRST  | 40     | 80     | ns    |
| IOR#/IOW# Command Width            | TCMDW | 120    |        | ns    |
| Write Data Setup to IOW# Rising    | TWDSU | 30     |        | ns    |
| Write Data Hold from IOW# Rising   | TWDHD | 15     |        | ns    |
| Read Access Time                   | TRAC  | 20     | 50     | ns    |
| Address Setup to IOR#/IOW# Falling | TASU  | 50     |        | ns    |
| Address Hold from IOR#/IOW# Rising | TAHD  | 30     |        | ns    |
| DACK# Setup to IOR#/IOW# Falling   | TDKSU | 40     |        | ns    |
| DACK# Hold from IOR#/IOW# Rising   | TDKHD | 160    |        | ns    |
| SD Hold from IOR# Rising           | TDHR  | 0      | 20     | ns    |
| DRQ Hold from IOR#/IOW# Falling    | TDRHD | 0      | 25     | ns    |

### 5.4.2 CD ROM/FM/Game Port Interface Timing

| Description  | Sym    | Min | Max | Units |
|--|--------|-----|-----|-------|
| SA to CA Delay   | TCA    | 3   | 20  | ns    |
| SA to XCS#/FMCS#/MIXCS#  | TXCS   | 5   | 20  | ns    |
| SD to XD Delay   | TXD    | 5   | 30  | ns    |
| XD to SD Delay   | TXSD   | 5   | 30  | ns    |
| XD Read Data Hold  | TXDH   | 5   |     | ns    |
| IOR#/IOW# to XIOR#/XIOW# Delay<br>IOR#/IOW# to GPR#/GPW# Delay | TCMIDD | 3   | 20  | ns    |
| IOW# to XD Enable Delay  | TXDE   | 5   | 20  | ns    |
| XDRQ to DRQ# Delay   | TDRQ   | 5   | 20  | ns    |
| DACK# to XDAK# Delay   | TXDAK  | 5   | 20  | ns    |

### 5.4.3 AD1848 Interface Timimg

| Description                  | Sym   | Min | Max | Units |
|------------------------------|-------|-----|-----|-------|
| SA to SPCS# Delay            | TSPCS | 5   | 20  | ns    |
| SD to SPD Delay              | TSPD  | 5   | 25  | ns    |
| SPD to SD Delay              | TSPSD | 5   | 20  | ns    |
| SPD Read Data Hold           | TSPDH | 5   |     | ns    |
| IOR#/IOW# to SPR#/SPW# Delay | TSPW  | 3   | 20  | ns    |
| IOW# to SPD Enable Delay     | TSPDE | 5   | 20  | ns    |

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## 5.4.3 AD1848 Interface Timimg (cont.)

| Description                      | Sym   | Min | Max | Units |
|----------------------------------|-------|-----|-----|-------|
| IOW# rising to SPD Disable Delay | τSPDN | 10  | 40  | ns    |
| DACK# to PDAK#/CDAK# Delay       | TXDAK | 5   | 20  | ns    |

## 5.5 DC Electrical Characteristics

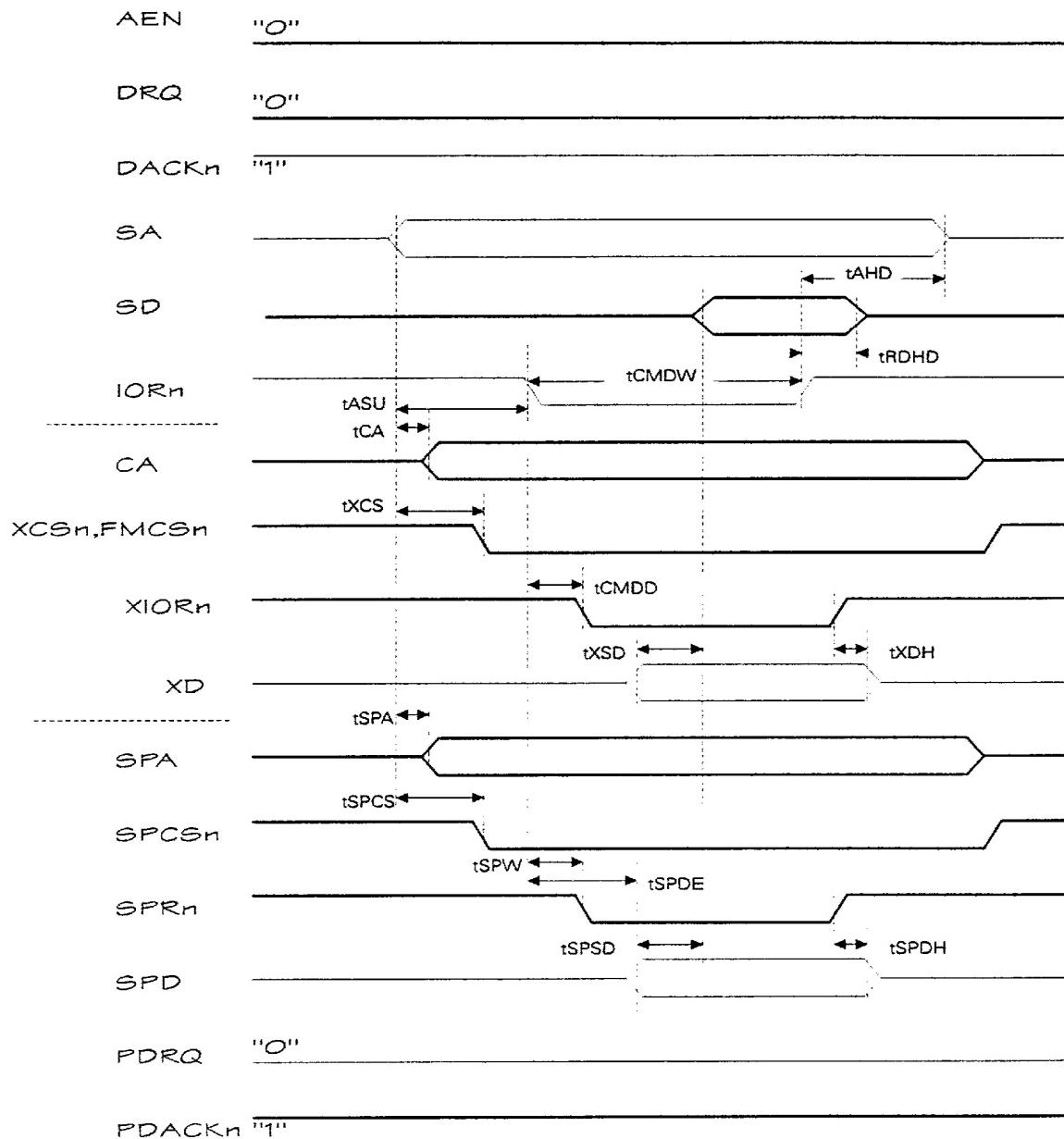
| Description                                     | Sym  | Min     | Max       | Units | Conditions              |
|---|------|---------|-----------|-------|-------------------------|
| Operating Supply Voltage                        | Vcc  | 4.5     | 5.5       | V     |                         |
| High Level Input Voltage                        | VIH  | 2.4     | Vcc + 0.3 | V     | Vcc = min               |
| High Level Input Voltage for RESET              | VIHa | 3.5     | Vcc + 0.3 | V     | Vcc = min               |
| Low Level Input Voltage                         | Vil  | -0.3    | 0.8       | V     | Vcc = max               |
| High Level Output Voltage                       | VOH  | Vcc-0.5 | Vcc       | V     | IOH = -4mA<br>VCC = max |
| Low Level Output Voltage                        | VOL  |         | 0.2       | V     | IOL = 4mA<br>VCC = min  |
| Input Leakage Current                           | IIl  |         | 10        | uA    | VCC = max               |
| Input Leakage Current with 5K pull-up resistor  | IIlA | -100    | -500      | uA    | VIN = 0V                |
| Input Leakage Current with 50K pull-up resistor | IIlb | -10     | -50       | uA    | VIN = 0V                |
| Output Leakage Current                          | IOl  |         | 10        | uA    | Vcc = max               |
| Static or Power-down Mode Current               | IPD  |         | 300       | uA    | Vcc = max               |

## 5.6 Absolute Maximum Ratings

| Description                   | Sym | Min  | Max  | Units | Conditions |
|-------------------------------|-----|------|------|-------|------------|
| Supply Voltage                | Vcc | -0.3 | 7.0  | V     |            |
| Storage Temperature           | TS  | -65  | +125 | C     |            |
| Ambient Operating Temperature | Ta  | -45  | +85  | C     |            |

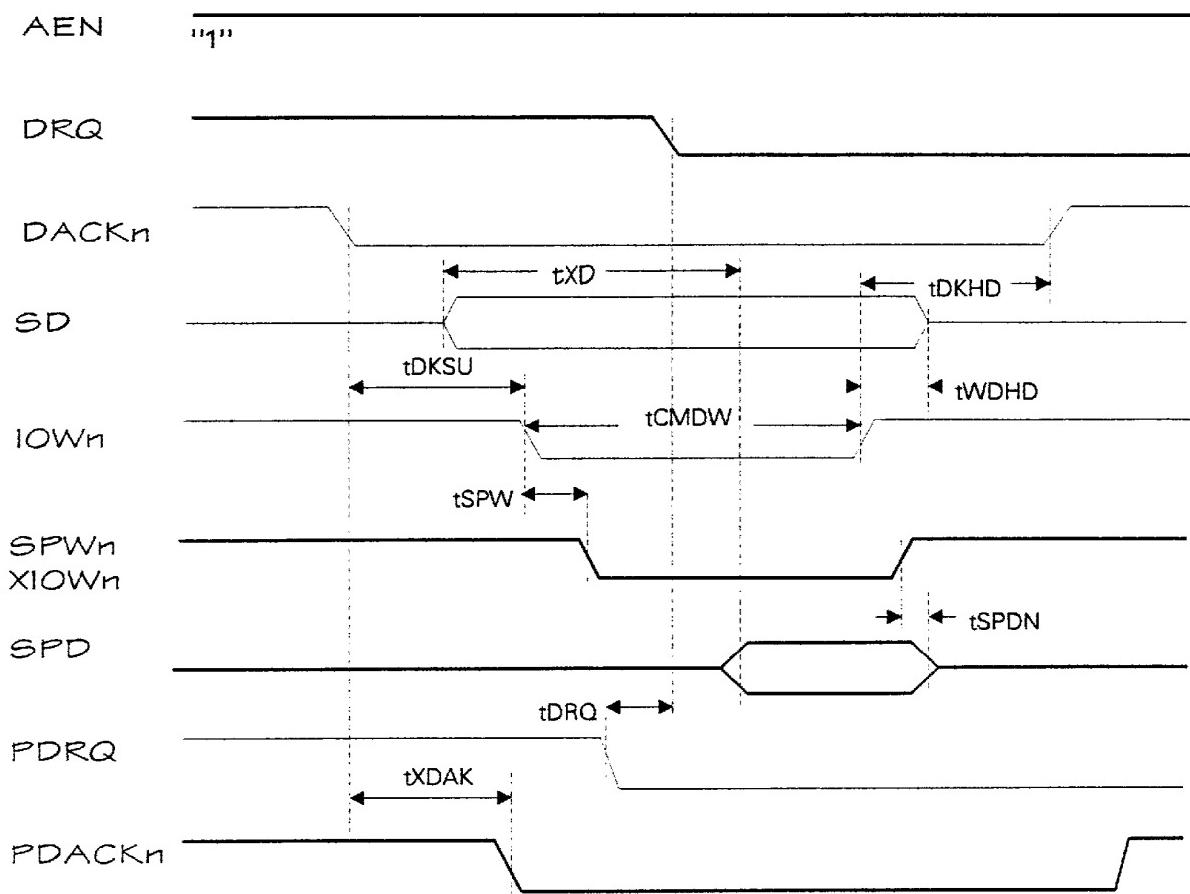
## 5.7 Timing Characteristics

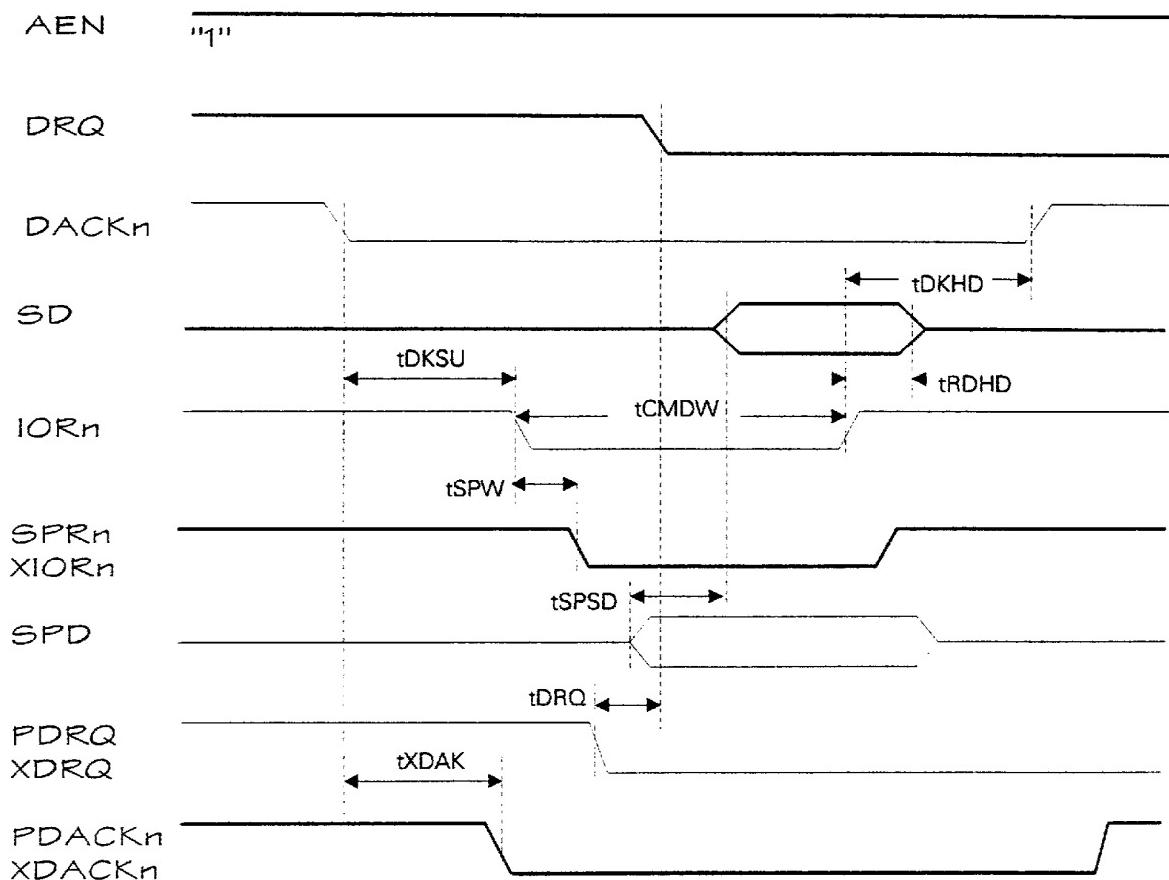
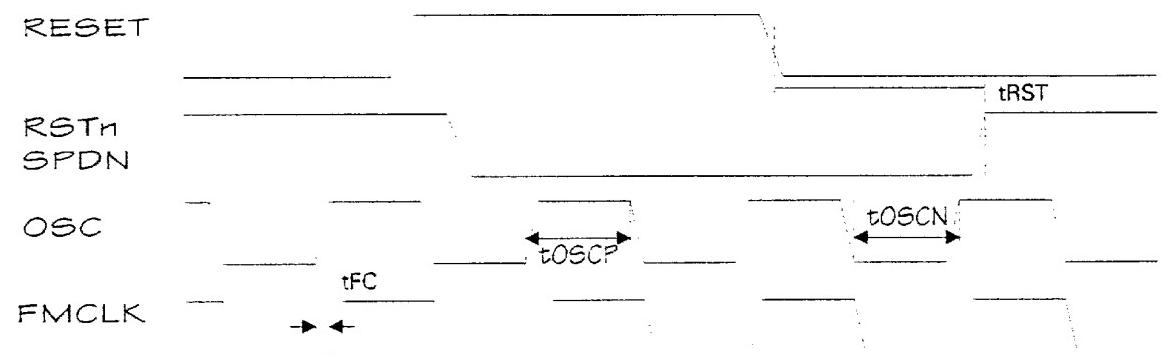
Figure 5-1 Register/CD/FM/Mixer/Sound Port IO Read Cycle



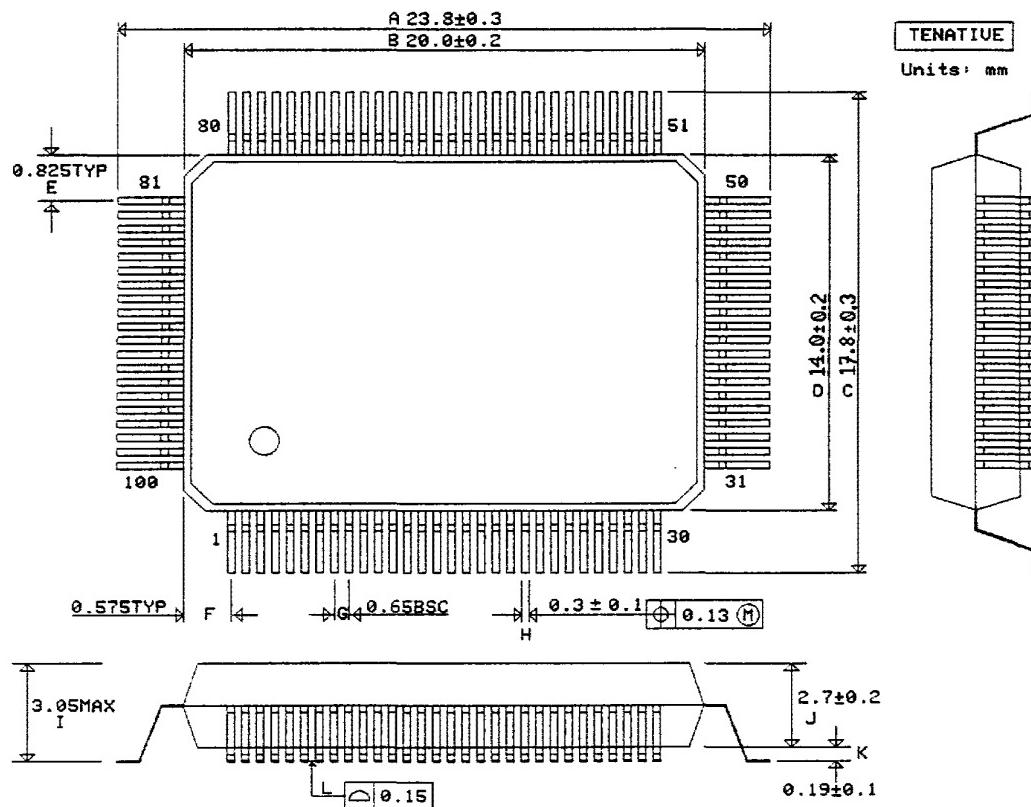
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Figure 5-2 DMA Write/Playback Cycle



**Figure 5-3 DMA Read/Capture Cycle****Figure 5-4 RESET and CLK Timing**

## 6.0 Mechanical Package



| DIM | MILLIMETERS |            | INCHES |        | DESCRIPTION                        |
|-----|-------------|------------|--------|--------|------------------------------------|
|     | MIN         | MAX        | MIN    | MAX    |                                    |
| A   | 23.5        | 24.1       | .925"  | .949"  | Maximum Width LEAD TO LEAD         |
| B   | 19.8        | 20.2       | .779"  | .795"  | Maximum Width PACKAGE ENVELOPE     |
| C   | 17.5        | 18.1       | .689"  | .713"  | Maximum Height LEAD TO LEAD        |
| D   | 13.8        | 14.2       | .543"  | .559"  | Maximum Height PACKAGE ENVELOPE    |
| E   | 0.825 TYP   | 0.825" TYP |        |        | LEAD CENTER TO PERP. LEAD PLANE    |
| F   | 0.575 TYP   | 0.226" TYP |        |        | LEAD CENTER TO PERP. LEAD PLANE    |
| G   | 0.65 BSC    | 0.256" BSC |        |        | LEAD TO LEAD CENTER SPACING        |
| H   | 0.2         | 0.4        | .008"  | .016"  | LEAD WIDTH                         |
| I   | —           | 3.05       | —      | .120"  | PACKAGE HEIGHT LEAD PLANE TO TOP   |
| J   | 2.5         | 2.9        | .098"  | .114"  | MAXIMUM THICKNESS PACKAGE ENVELOPE |
| K   | 0.09        | 0.29       | .0035" | .0114" | LEAD PLANE TO PACKAGE BOTTOM       |
| L   | —           | 0.15       | —      | .006"  | LEAD PLANE SKEW                    |
| M   | 0.1         | 0.25       | .004"  | .010"  | LEAD THICKNESS                     |
| N   | 0.6         | 1.0        | .024"  | .039"  | LEAD FOOTPRINT                     |

